**ALLEGATO A**

**Struttura corso “IC Layout Designer (technician level)”**

**Conoscenze**

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| **INSEGNAMENTO** | **DURATA** | **MODALITA’** |
| Knowledge of OFFICE package (Excel, Word, Power Point) focused on data analysis, reporting and internal communication | 4h Classroom  8h Lab | Classroom/Laboratory |
| Fundamentals of UNIX System | 4h | Classroom |
| Basic principles of electric circuit theory (e.g. voltage, current, capacitors, inductors, resistors, Ohm's law, Kirchhoff's laws) | 40h | Classroom |
| Knowledge of main active and passive electronic components (e.g. transistors, diodes, integrated capacitors and resistors) | 40h | Classroom |
| Basic knowledge of the manufacturing technologies for semiconductor integrated electronic circuits | 40h | Classroom |
| Knowledge and familiarity with the development flow of an integrated circuit | 8h | Classroom |
| Knowledge of the software for the design and layout of semiconductor integrated electronic circuits (EDA tools) and its use to translate the schematic of the integrated electronic circuit into the corresponding layout | 20h Classroom  140h Lab | Classroom/Laboratory |
| Knowledge of the software for layout verification (Calibre) | 4h Classroom  16h Lab | Classroom/Laboratory |
| Knowledge of the layout verification flow (DRC, LVS, parasitic extraction, RDSON extraction) | 4h Classroom  16h Lab | Classroom/Laboratory |
| Introduction to the design related aspects of the layout (matching, parasitic resistance, parasitic capacitance) | 20h Classroom  20h Lab | Classroom/Laboratory |
| Knowledge of basic risks related to job activities | 8h | Classroom |
| Fundamentals of labour contracts | 8h | Classroom |
| Acquisition, through supervised training and internship in one of the partner companies, of the practical skills necessary to carry out the specific tasks of the layout designer | 120h | Companies |

**Competenze**

• Knowing how to translate the schematic of the integrated electronic circuit provided by the electronic engineers, into its corresponding layout using suitable CAD software

• Understanding and interpreting the design requirements provided by electronic engineers, ensuring that the circuit design meets all technical and functional specifications

• Understanding, interpreting, and applying the rules indicated in the Design rule manuals of the manufacturing process technology selected for the project

**Suddivisione oraria**

**400** ore di formazione teorico-pratica, di cui **200** ore di aula e **200** ore di laboratorio  
**120** ore di tirocinio curriculare  
= **520 ORE TOTALI**

**Soggetto attuatore**

Dipartimento di Ingegneria Elettronica dell’Università di Pavia, per conto di Fondazione Alma Mater Ticinensis.